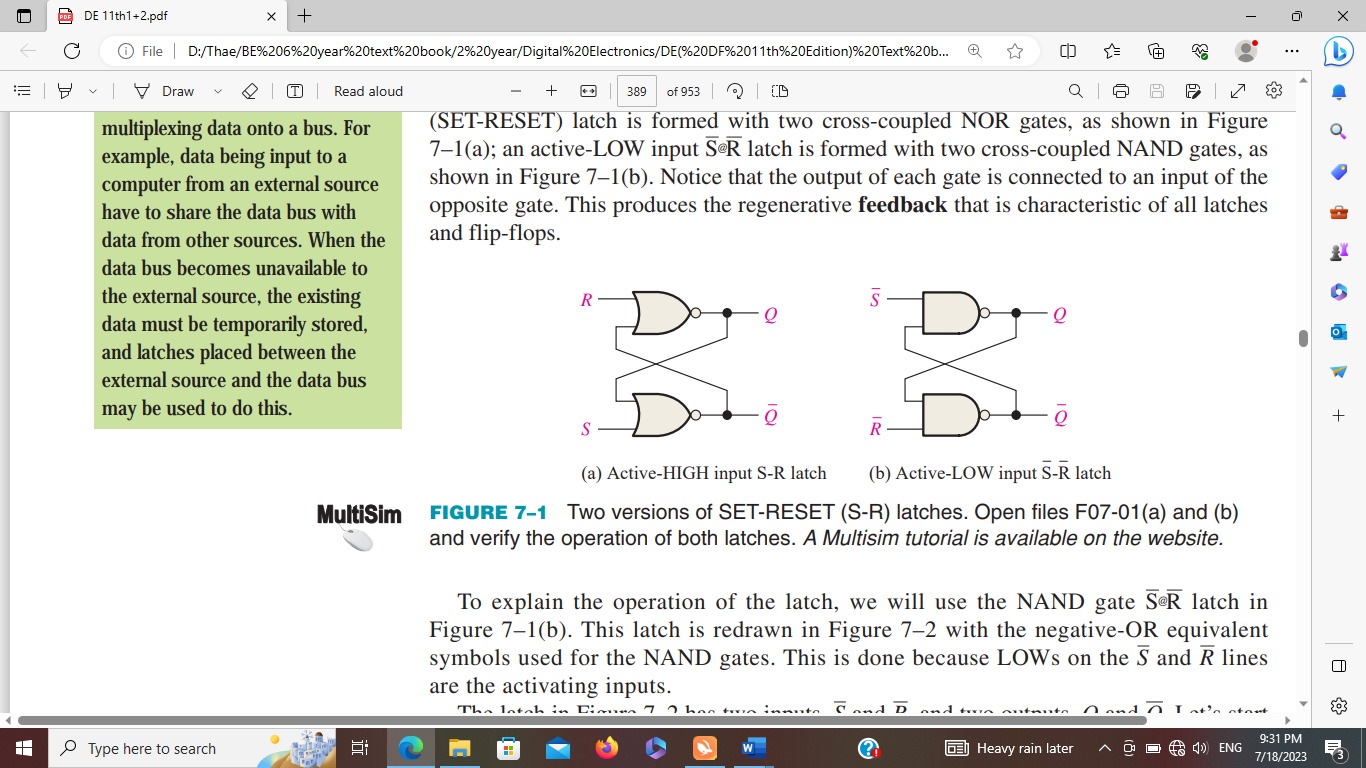
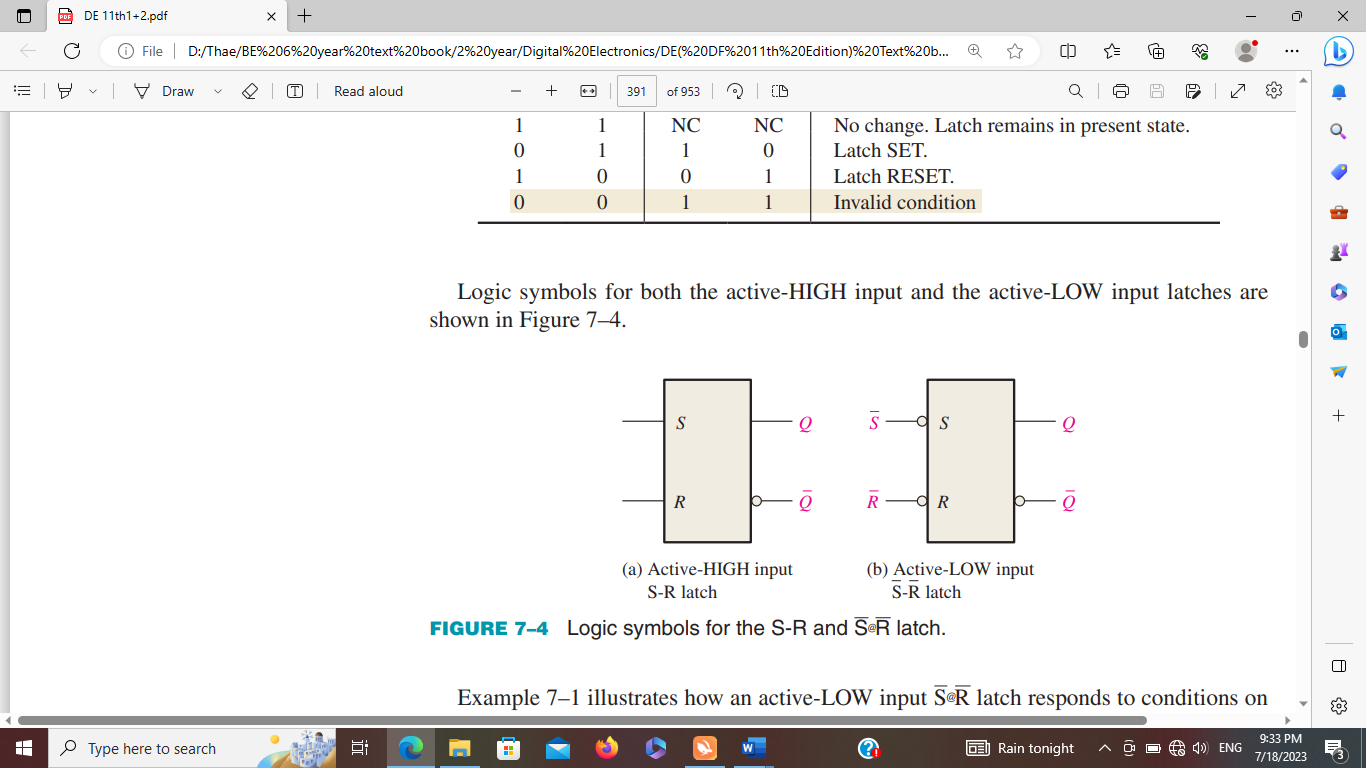
**Chapter 7**

1. Draw the logic diagram, logic symbol and truth table for the active LOW input - latch.

**Solution**

logic diagram logic symbol

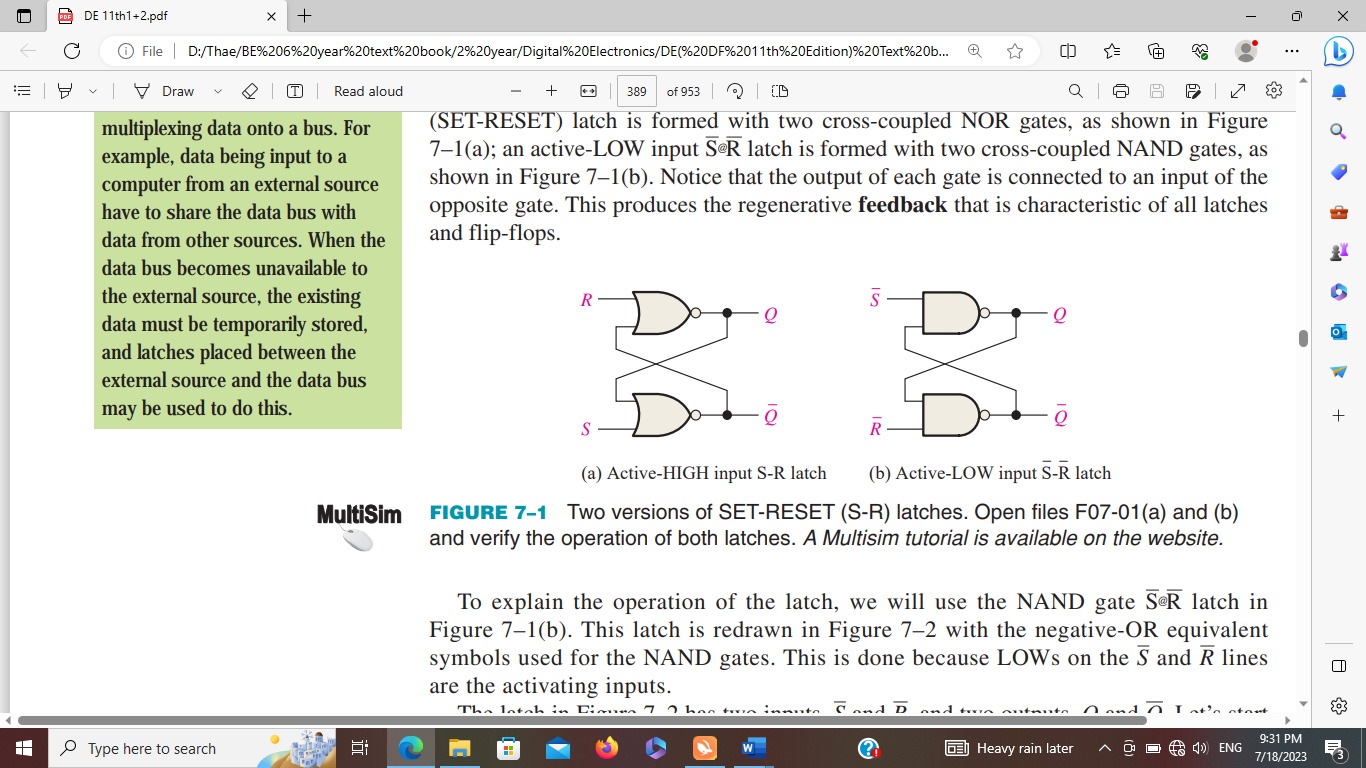
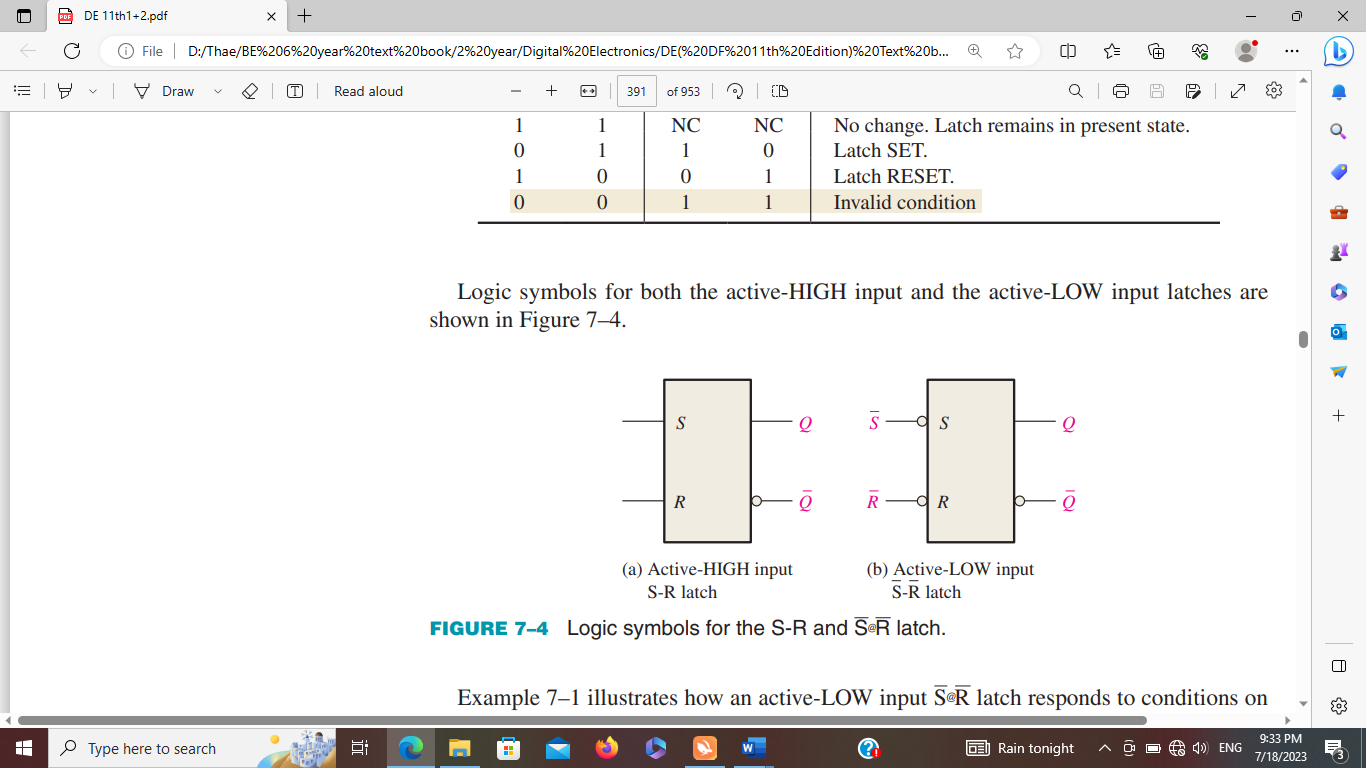
|  |  |  |  |
| --- | --- | --- | --- |
| Inputs | | Outputs | |
|  |  | Q |  |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | NC | NC |

Truth Table

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2. Draw the logic diagram, logic symbol and truth table for the active HIGH input - latch.

**Solution**

logic diagram logic symbol

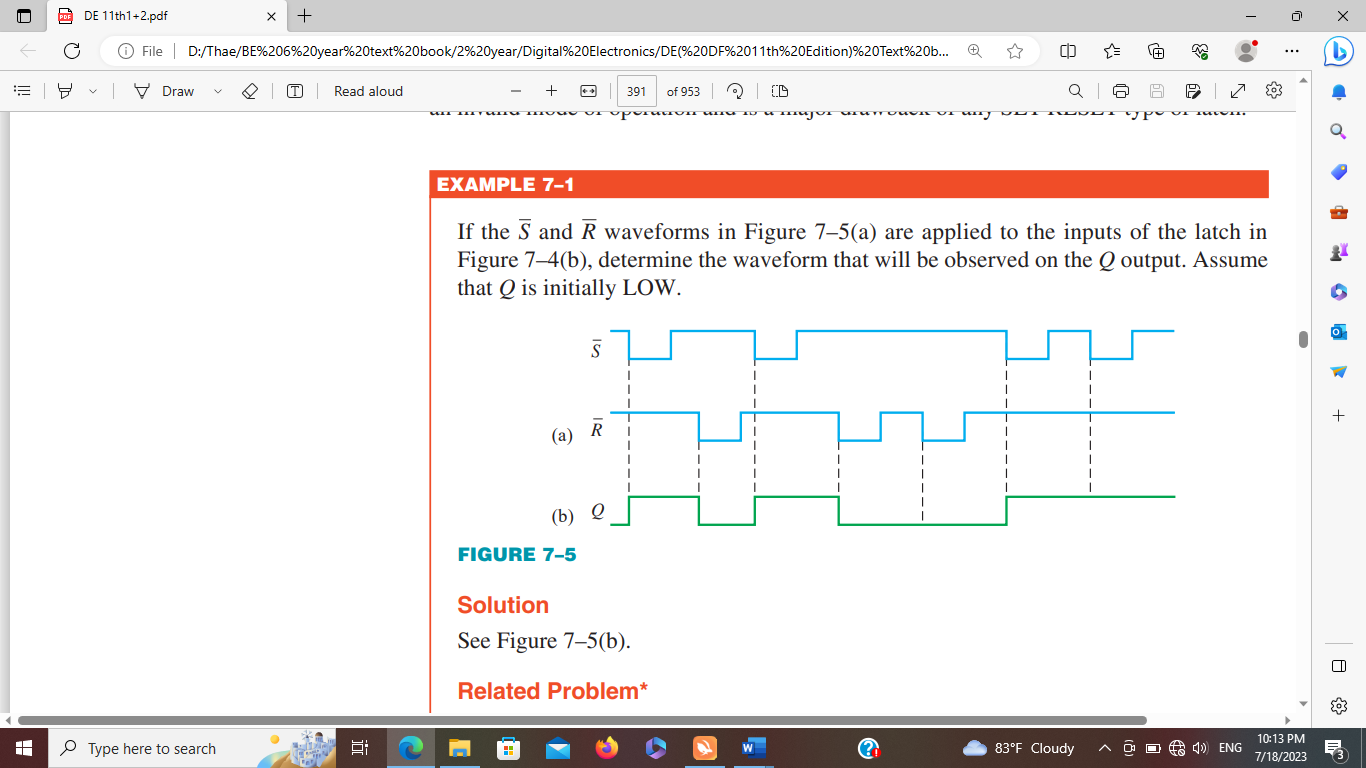
|  |  |  |  |
| --- | --- | --- | --- |
| Inputs | | Outputs | |
| S | R | Q |  |
| 0 | 0 | NC | NC |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 |

Truth Table

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3. Determine the Q output of an active-LOW input - latch if the waveforms in Figure.

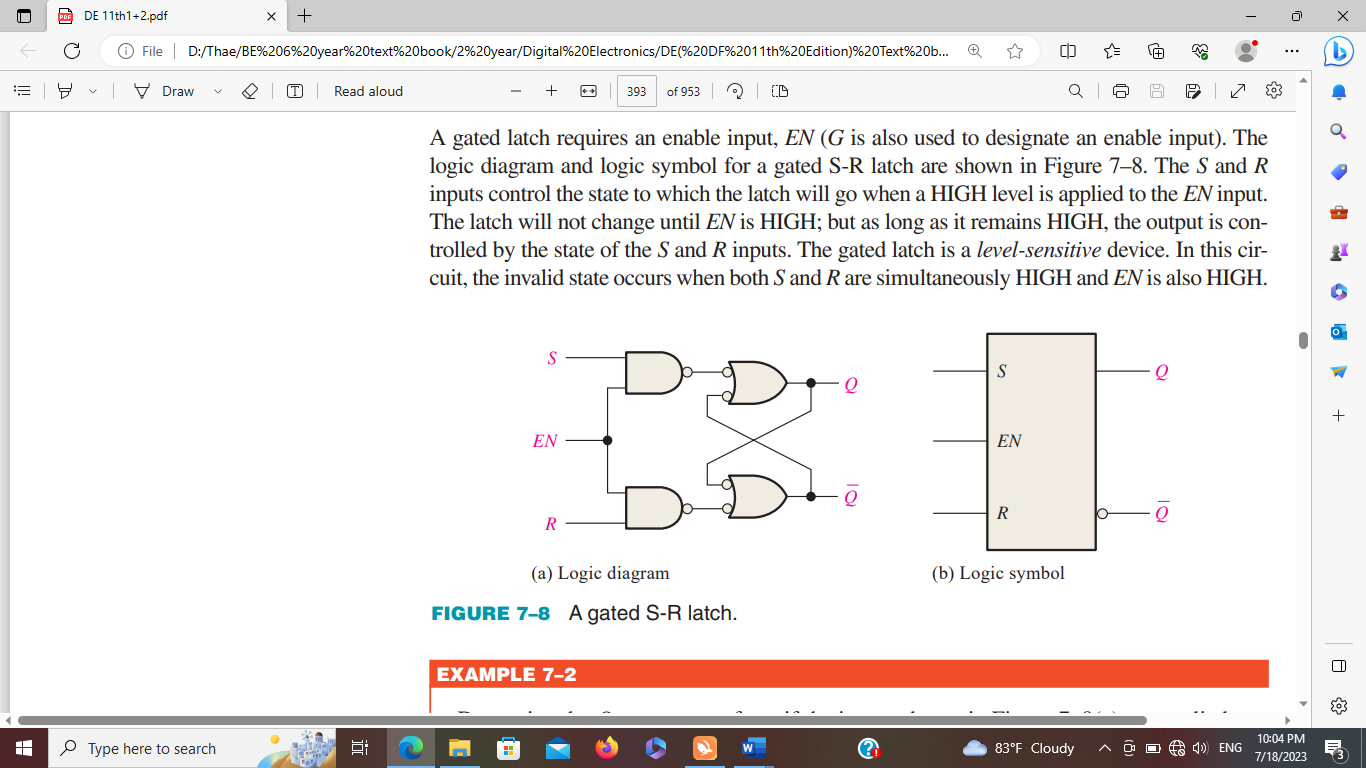
**Solution**



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4. Draw the logic diagram, logic symbol and truth table for the gated S-R latch.

**Solution**



|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Inputs | | | Outputs | |
| EN S | | R | Q |  |
| 0 | X | X | NC | NC |
| 1 | 0 | 0 | NC | NC |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |

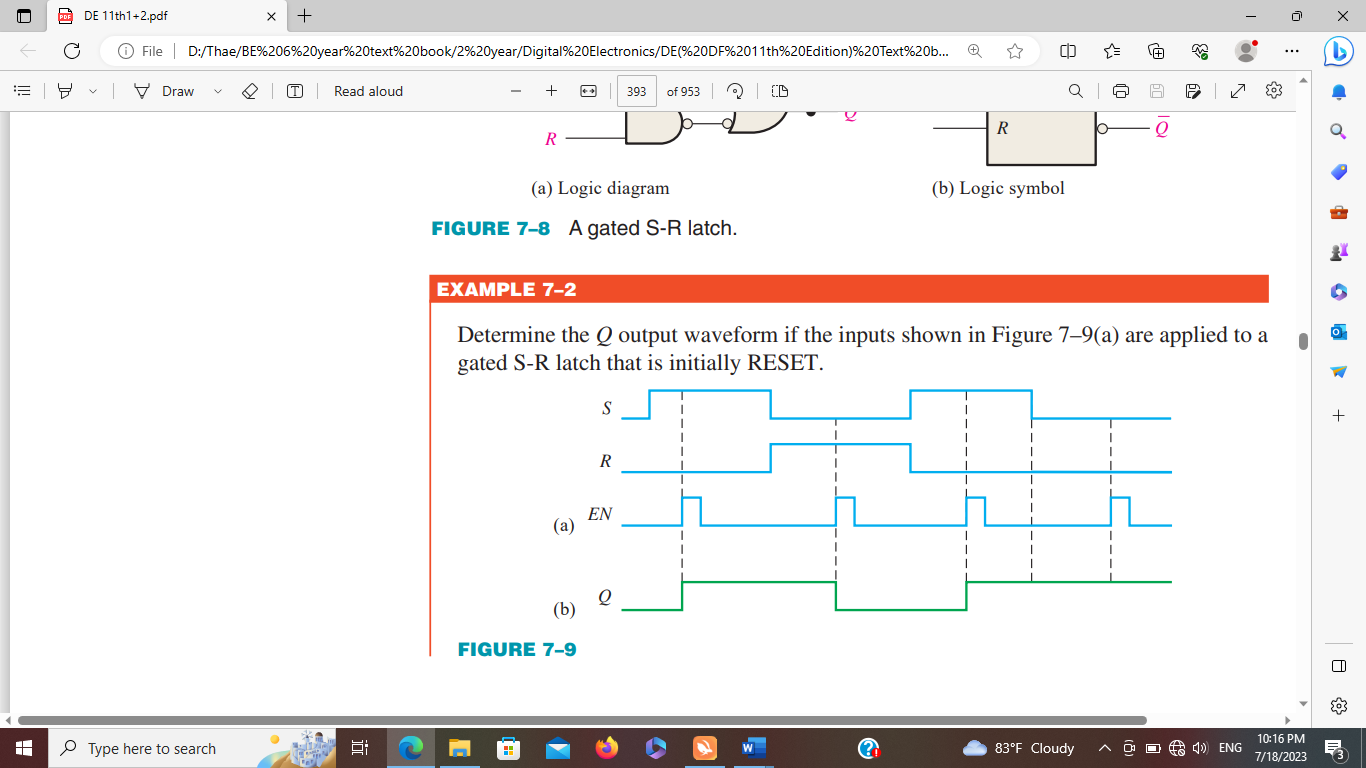
Truth Table

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5. Determine the *Q* output waveform if the inputs shown in Figure are applied to a gated S-R latch that is

initially RESET.

**Solution**

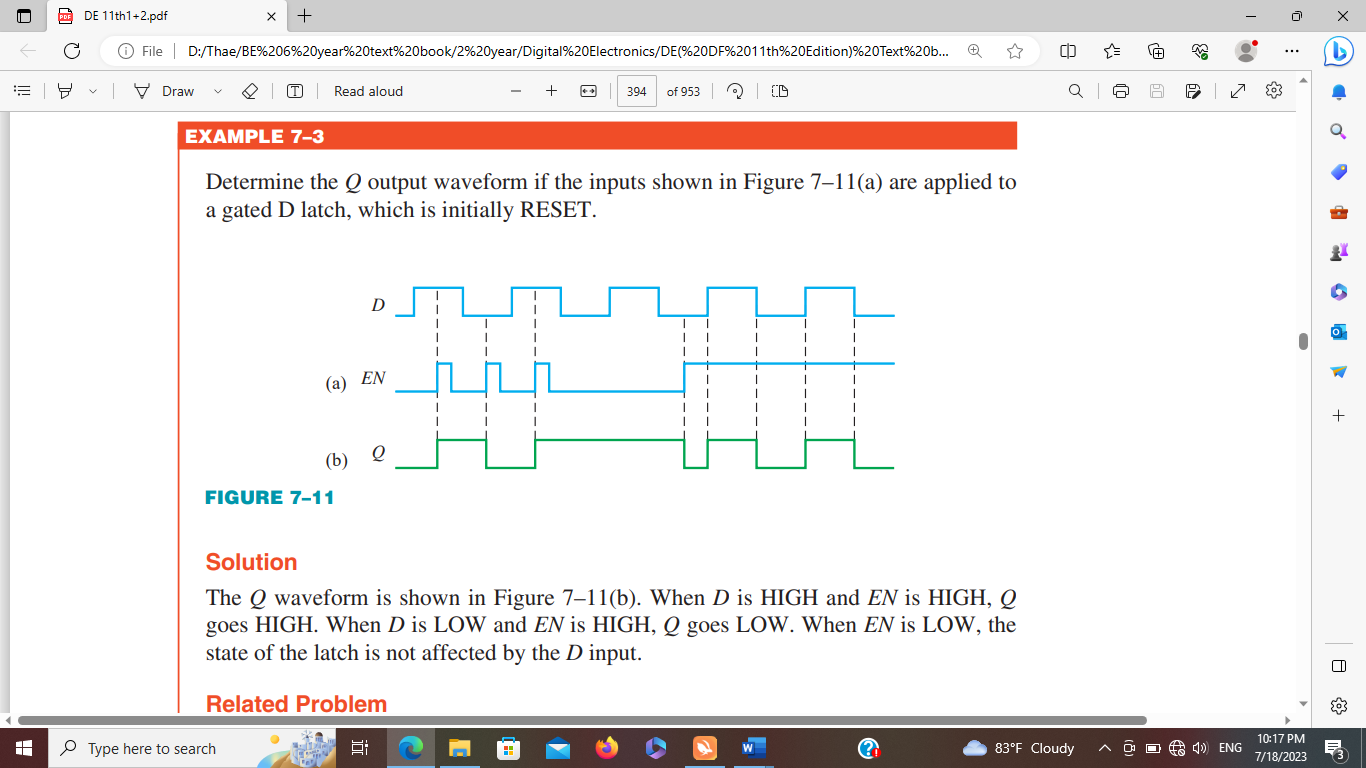


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6. Determine the *Q* output waveform if the inputs shown in Figure are applied to a gated D latch, which is

initially RESET.

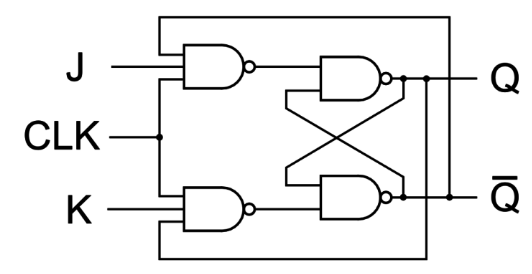
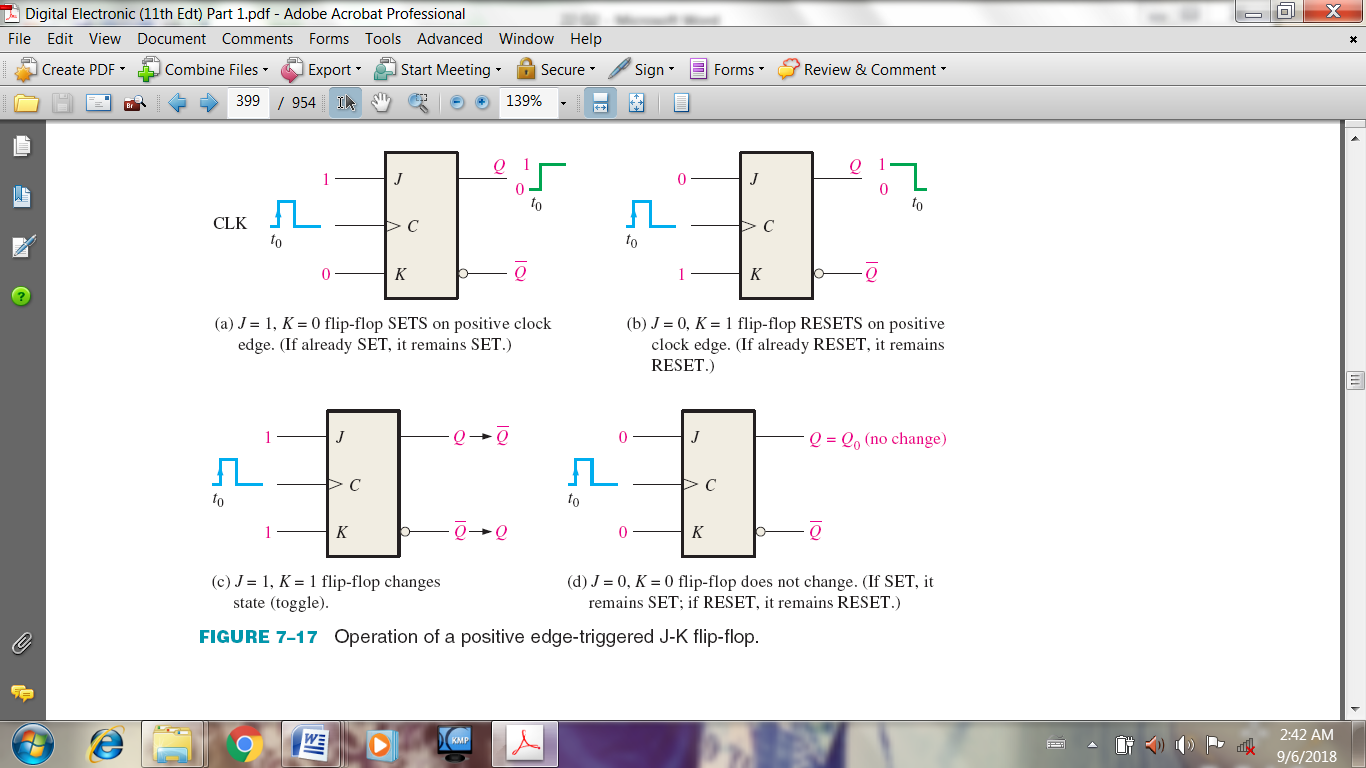
**Solution**



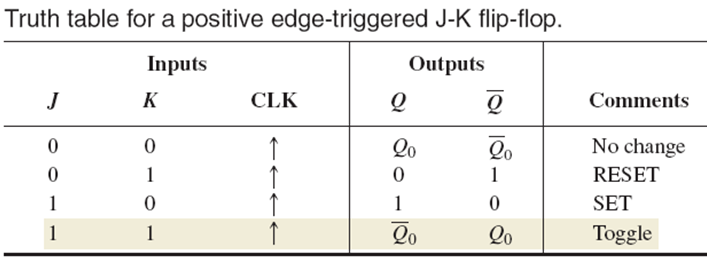
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7. Draw the logic diagram, logic symbol and truth table for J-K flip flop.

**Solution**

logic diagram logic symbol



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8. Draw the Q outputs for the positive and negative edge triggered J-K flip-flops. The J, K and clock input

are shown in Figure. Assume Q outputs are initially LOW.

**Solution**

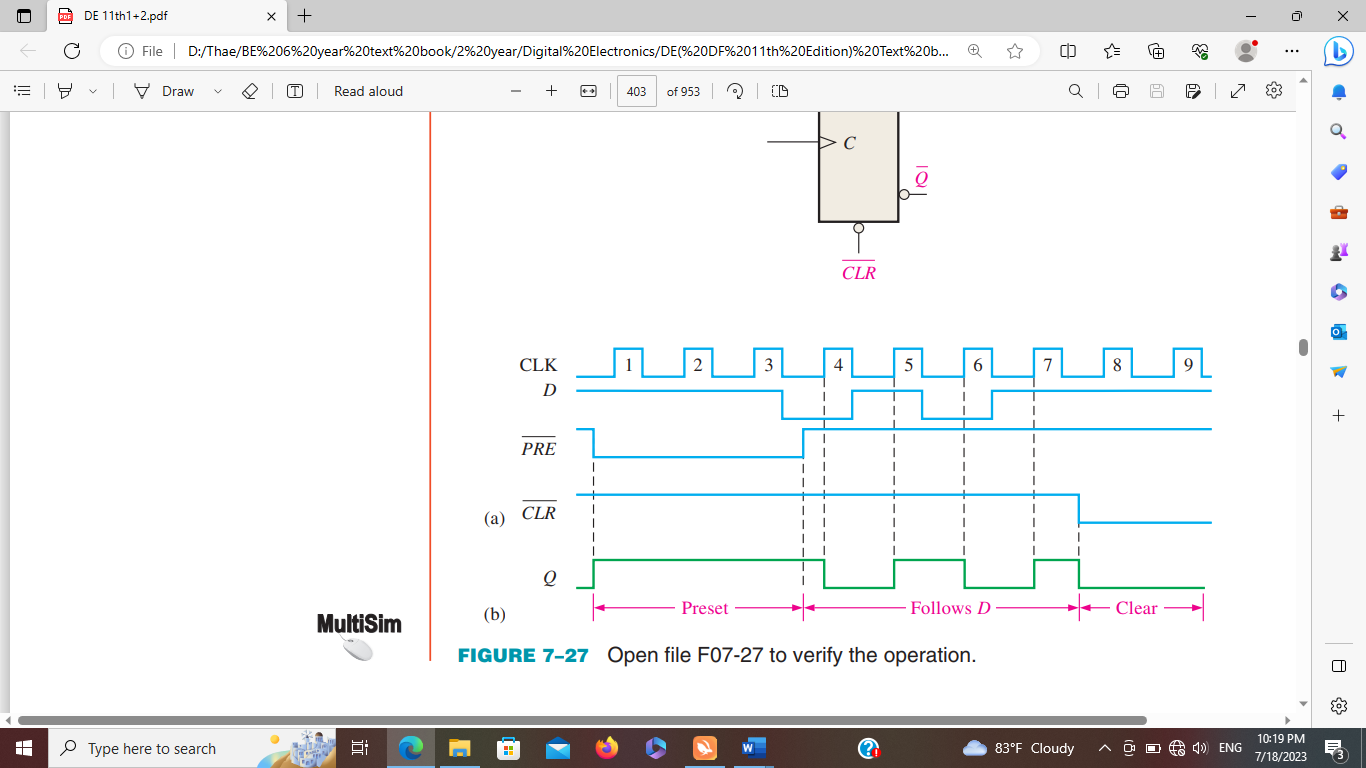


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9. For the positive edge-triggered D flip-flop with preset and clear inputs in figure, determine the Q output

for the following timing diagram if *Q* is initially LOW.

**Solution**



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10. For the positive edge triggered D flip-flop which is one part of 74HC74 with preset and clear input in Figure, determine the Q output if Q is RESET.

**Solution**

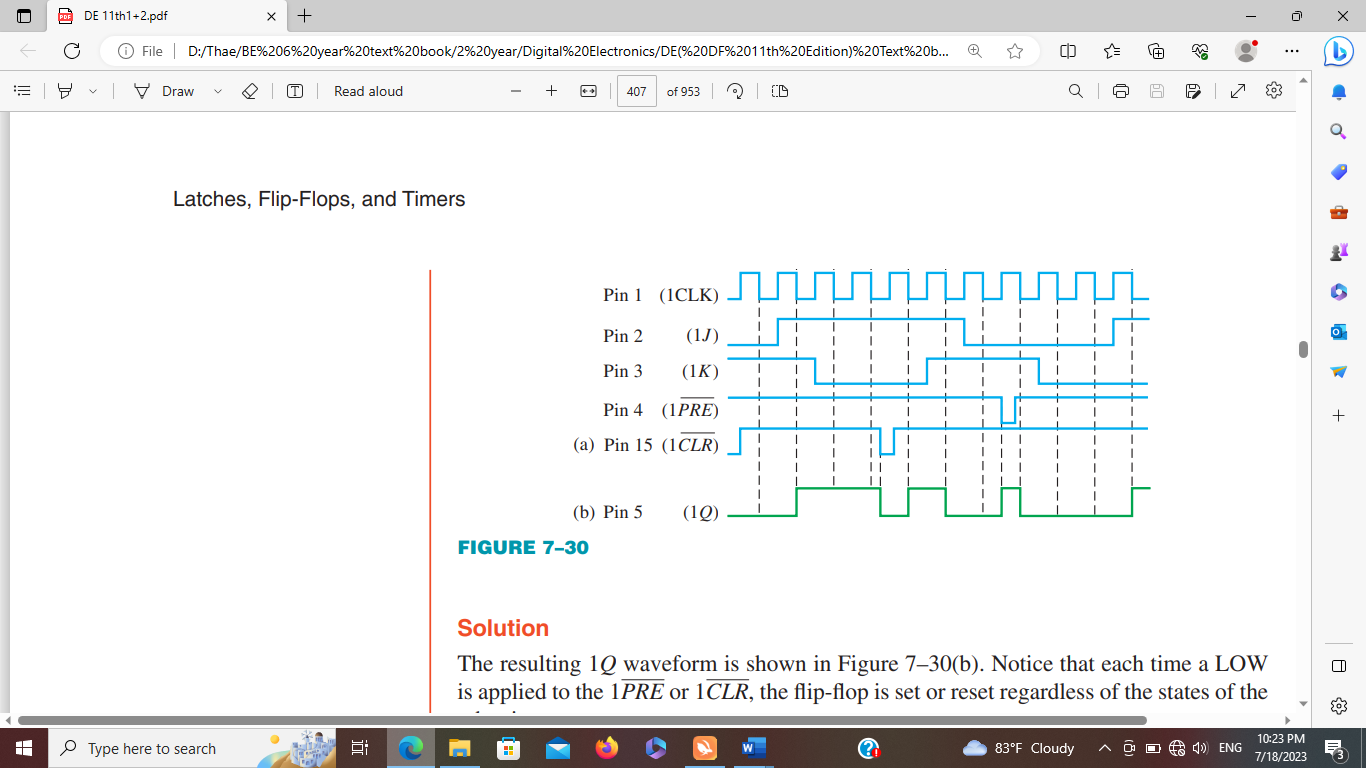


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11. The 1J, 1K, 1CLK, , and waveforms in Figure are applied to one of the negative edge-

triggered flip-flops in a 74HC112 package. Determine the 1Q output waveform.

**Solution**



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12. The 2J, 2K, 2CLK, , and waveforms in figure are applied to one of the negative edge-triggered flip flop in a 74HC112 package. Determine the 2Q output waveform.

**Solution**



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13. Draw the internal functional diagram of a 555 timer with pin numbers. And then, name the two modes which it can be used.

**Solution**

* Name the two modes which it can be used are monostable and astable.



Internal functional diagram of a 555 timer with pin numbers

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14. A 555 timer is configured to run as multivibrator as shown in figure. Determine its frequency and duty cycle. If a diode is connected across R2, determine the duty cycle.



**Solution**

R1 = 2 kΩ, R2 = 4.3 kΩ, C1 = 0.1µF, f=?, Duty cycle = ?

f = 1.44/ (R1 + 2R2)C1

= 1.44/ (2k+ 2(4.3k)) 0.1µ

= 1.4 kHz

Duty cycle =

=

=

= 59.43%

If the diode D1 is connected across R2,

Duty cycle=

=

= 31.75%

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15. Determine the value of REXT that will produce a pulse width of 5µs when connected to a 74LS122. Show

the connections. Assume CEXT = 560 pF.

**Solution**

tw = 5µs

Assume CEXT = 560pf

tw = 0.32 REXT CEXT (1+ )

REXT = - 0.7 = 27.9 kΩ

REXT = 27 kΩ (std. value)



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16. An output pulse of 100 ms duration is to be generated by a 74121 one-shot. Using a capacitor of 3.3 µF,

determine the value of external resistance required.

**Solution**

tW = 100ms , CEXT =3.3µF

tW = 0.7REXTCEXT

REXT =tW / 0.7CEXT

REXT =100ms / 0.73.3µF = 43.29 kΩ

REXT = 43 kΩ (std. value)

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17. Determine the values of the external resistors for a 555 timer used as an astable multivibrator with an

output frequency of 10 kHz, if the external capacitor C is 0.004µF and the duty cycle is to be approximately 80%.

**Solution**

C1 = 0.004µF, f=10 kHz, Duty cycle = 80%, R1 =? R2=?

f = 1.44/ (R1 + 2R2) C1

10 k =1.44/ (R1 + 2R2)0.004 µ

R1 + 2R2 = 36 kΩ ............... (1)

Duty cycle=

80% =

= 0.8

R1 + 2R2  = ............... (2)

R1 = 21.6 kΩ = 22 kΩ (std.val)

R2 = 7.2 kΩ = 7.5 kΩ (std.val)

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